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# UNITED STATES PATENT APPLICATION

**OF**

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**FOR**

# APPARATUS FOR APPLYING OFF-STATE STRESS TO P-MOS DEVICE

**[0001]** This application claims the benefit of Korean Patent Application No. 2002-58286, filed on September 26, 2002, which is hereby incorporated by reference for all purposes as if fully set forth herein.

## BACKGROUND OF THE INVENTION

### Field of the Invention

**[0002]** The present invention relates to a polycrystalline thin film transistor liquid crystal display device, and more particularly, to an apparatus for applying an OFF-state stress to a p-type polycrystalline thin film transistor for stabilization.

### Discussion of the Related Art

**[0003]** Until recently, cathode-ray tubes (CRTs) have generally been used for display systems. However, use of flat panel displays is becoming increasingly common because of their small depth, low weight, and low power consumption. Presently, thin-film transistor-liquid crystal displays (TFT-LCDs) are being developed that have high resolution, small depth and high color reproducibility.

**[0004]** When a pixel is turned on by a switching element, the pixel transmits light from a backlight unit. Amorphous silicon (a-Si:H) thin film transistors (TFT) that include a semiconductor layer of amorphous silicon are widely used as switching elements because the amorphous silicon thin film can be formed on a large-sized insulating substrate such as a glass substrate under a low temperature. However, even though TFT-LCDs using amorphous silicon TFTs have an advantage over CRTs of low power consumption, the price of TFT-LCDs is higher than that of CRTs because TFT-LCDs require an expensive driving circuit.

**[0005]** FIG. 1 is a schematic plane view of an amorphous silicon thin film transistor liquid crystal display device according to the related art.

**[0006]** In FIG. 1, a substrate 10 includes a display region "D." A gate driving integrated circuit (IC) 20 and a data driving IC 30 are formed between the display region "D" and a printed circuit board (PCB) 40. Generally, the gate and data driving ICs 20 and 30, which are referred to as a large scale integration (LSI), are fabricated by using single crystalline silicon and connected to the substrate by a tape automated bonding (TAB) method. However, as the resolution of the liquid crystal display (LCD) device increases, more leads are necessary to connect the substrate and the driving LSI. For example, in a super extended graphic array (SXGA) display having 1280 x 1024 x 3 pixels, at least 1280 x 3 x 1024 leads are required for connection. The process for fabricating large numbers of leads is complex, thereby reducing reliability and production yield. Moreover, the price of LCD devices increases due to the expensive driving LSI. To solve these problems, LCD devices using a polycrystalline silicon thin film transistor are suggested.

**[0007]** FIG. 2 is a schematic plane view of a polycrystalline silicon thin film transistor liquid crystal display device according to the related art.

**[0008]** In FIG. 2, a substrate 10 includes a display region "D." Contrary to LCD devices using an amorphous silicon thin film transistor, a gate driving circuit 22 and a data driving circuit 32 of the LCD device of FIG. 2 are directly formed on the substrate 10 using a polycrystalline silicon as a switching element of each pixel (not shown). Accordingly, an additional process of connecting the substrate and a driving LSI is not necessary.

**[0009]** FIG. 3 is a schematic cross-sectional view of a polycrystalline silicon thin film transistor according to the related art.

**[0010]** In FIG. 3, a first insulating layer (a buffer layer) 40 is formed on a substrate 10 and an active layer 42 of polycrystalline silicon is formed on the first insulating layer 40. A second insulating layer (a gate insulating layer) 44 is formed on the active layer 42 and a gate electrode 46 is formed on the second insulating layer 44 over the active layer 42. A third insulating layer (an interlayer insulating layer) 48 having contact holes is formed on the gate electrode 46. Source and drain electrodes 50a and 50b are formed on the third insulating layer 48 and connected to the active layer 46 through the contact holes. A fourth insulating layer (a passivation layer) 52 is formed on the source and drain electrodes 50a and 50b. A pixel electrode 54 is formed on the fourth insulating layer 52 and connected to the drain electrode 50b.

**[0011]** FIG. 4 is a schematic perspective view of a liquid crystal display device according to the related art.

**[0012]** In FIG. 4, first and second substrates face into and are spaced apart from each other, and a liquid crystal layer is interposed therebetween. The first substrate having a thin film transistor (TFT) "T" and array lines, and the second substrate having a black matrix and a color filter layer are fabricated through various process steps. Among the various process steps, a process for stabilizing the TFT "T" may be performed for the first substrate having the TFT "T" or for the attached first and second substrates, i.e. for a cell having the TFT "T."

**[0013]** When a polycrystalline silicon (p-Si) TFT-LCD device is driven for a long period of time under room temperature, carriers generated at a P-N (positive-negative) junction of the p-Si TFT produce an OFF-current ($I_{OFF}$) may leave residual images on the LCD device panel which can degrade the LCD device. Accordingly, a stabilizing process is

performed in which an OFF-state stress is applied to the P-type TFT to prevent the residual images. To apply an OFF-state stress means to apply a voltage opposite to or different from a normal voltage. Through this stabilizing process, the OFF-current may be reduced and a mobility of the TFT may be improved.

**[0014]** FIG. 5 is a schematic circuit diagram illustrating one pixel of a liquid crystal display device according to the related art.

**[0015]** In FIG. 5, a P-type thin film transistor (P-TFT) is formed in each pixel region. A gate electrode and a source electrode of the P-TFT are connected to a gate line 12 and a data line 14, respectively. A drain electrode of the P-TFT is connected to a storage capacitor "$C_{ST}$" and a liquid crystal capacitor "$C_{LC}$." The storage capacitor "$C_{ST}$" is connected to a common line 16, and the liquid crystal capacitor "$C_{LC}$" is connected to the common electrode 18.

**[0016]** FIGs. 6A and 6B are a schematic circuit diagram and a timing chart, respectively, illustrating a stabilizing method including a first OFF-state stress applied to a liquid crystal display device according to the related art.

**[0017]** In FIGs. 6A and 6B, when a low gate voltage (for example, -10V) is applied to a gate electrode of a P-TFT through a gate line 12, the P-TFT is turned ON. Since a low data voltage (for example, -10V) is applied to a source electrode of the P-TFT through a data line 14, the low data voltage is also applied to a drain electrode of the P-TFT. After the low data voltage is applied to the drain electrode of the P-TFT, a high gate voltage (for example, 30V) is applied to the gate electrode of the P-TFT, thereby turning OFF the P-TFT. Then, a high data voltage (for example, 0V) is applied to the source electrode of the P-TFT. Since the drain electrode maintains the low data voltage and the P-TFT maintains a turn-OFF

state, a first OFF-state stress including the high gate voltage of the gate electrode, the high data voltage of the source electrode and the low data voltage of the drain electrode is obtained as a forward bias mode.

**[0018]** FIG. 6C is a schematic cross-sectional view illustrating an effect of a first OFF-state stress of a stabilizing method according to the related art.

**[0019]** In FIG. 6C, since a voltage difference (for example, 40V) between a gate electrode and a drain electrode is higher than that between the gate electrode and a source electrode, an electric field between the gate electrode and the drain electrode is higher and becomes dominant. Accordingly, electrons adjacent to the drain electrode are accelerated by the electric field and captured by an interface of a polycrystalline silicon layer and a trap in the polycrystalline silicon grain boundary. The captured electrons cure the interface and the trap of the polycrystalline silicon layer adjacent to the drain electrode.

**[0020]** FIG. 6D is a current-voltage (I-V) curve illustrating an OFF-current of a P-TFT after a first OFF-state stress of a stabilizing method according to the related art.

**[0021]** In FIG. 6D, an OFF-current of a P-TFT is improved after a first OFF-state stress is applied to the P-TFT because defects of the P-TFT are cured.

**[0022]** FIGs. 7A and 7B are a schematic circuit diagram and a timing chart illustrating a stabilizing method including a second OFF-state stress applied to a liquid crystal display device according to the related art, respectively.

**[0023]** In FIGs. 7A and 7B, when a low gate voltage (for example, -10V) is applied to a gate electrode of a P-TFT through a gate line 12, the P-TFT is turned ON. Since a high data voltage (for example, 0V) is applied to a source electrode of the P-TFT through a data line 14, the high data voltage is also applied to a drain electrode of the P-TFT. After the

high data voltage is applied to the drain electrode of the P-TFT, a high gate voltage (for example, 30V) is applied to the gate electrode of the P-TFT, thereby turning OFF the P-TFT. Then, a low data voltage (for example, -10V) is applied to the source electrode of the P-TFT. Since the drain electrode maintains the high data voltage and the P-TFT maintains a turn-OFF state, a second OFF-state stress including the high gate voltage of the gate electrode, the low data voltage of the source electrode and the high data voltage of the drain electrode is obtained as a reverse bias mode.

**[0024]** FIG. 7C is a schematic cross-sectional view illustrating an effect of a second OFF-state stress of a stabilizing method according to the related art.

**[0025]** In FIG. 7C, since a voltage difference (for example, 40V) between a gate electrode and a source electrode is higher than that between the gate electrode and a drain electrode, an electric field between the gate electrode and the source electrode is higher and becomes dominant. Accordingly, electrons adjacent to the source electrode are accelerated by the electric field and captured by an interface of a polycrystalline silicon layer and a trap in the polycrystalline silicon grain boundary. The captured electrons cure the interface and the trap of the polycrystalline silicon layer adjacent to the source electrode.

**[0026]** FIG. 7D is a current-voltage (I-V) curve illustrating an OFF-current of a P-TFT after a second OFF-state stress of a stabilizing method according to the related art.

**[0027]** In FIG. 7D, an OFF-current of a P-TFT is improved after a second OFF-state stress is applied to the P-TFT because defects of the P-TFT are cured. Moreover, an ON-current is also improved.

**[0028]** In a stabilizing method including an OFF-state stress, a gate voltage having two values and a data voltage having two values are used to improve a P-TFT

property by reducing an OFF-current. However, since forward and reverse modes are alternated, the stabilizing method is complex. Moreover, when many LCD cells are fabricated in one substrate, the stabilizing method is performed for each LCD cell. Accordingly, it takes much time to perform the stabilizing method, thereby reducing production yield.

## SUMMARY OF THE INVENTION

**[0029]** Accordingly, the present invention is directed to an apparatus for applying an OFF-state stress to a liquid crystal display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

**[0030]** An advantage of the present invention is that it provides an apparatus for applying an OFF-state stress to a p-type thin film transistor to improve OFF-current and mobility.

**[0031]** Another advantage of the present invention is that it provides an apparatus for applying an OFF-state stress to a plurality of cells at the same time so as to improve production yield.

**[0032]** Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

**[0033]** To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an apparatus for applying an

OFF-state stress to a P-MOS device of one of an array substrate for an LCD device and an LCD panel having attached substrates includes: a power supply unit supplying a source power; a panel loading unit including a plurality of panel jigs on which one of the array substrate and the LCD panel is loaded; a voltage control unit including a plurality of voltage control channels and modulating a voltage of the source power; a frequency control unit including a plurality of frequency control channels and modulating a frequency of the source power; a time setting unit determining a time period of supplying the source power; and a panel selecting unit including a plurality of panel selecting channels and modulating an application of the source power.

**[0034]** It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0035]** The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

**[0036]** In the drawings:

**[0037]** FIG. 1 is a schematic plane view of an amorphous silicon thin film transistor liquid crystal display device according to the related art;

**[0038]** FIG. 2 is a schematic plane view of a polycrystalline silicon thin film transistor liquid crystal display device according to the related art;

**[0039]** FIG. 3 is a schematic cross-sectional view of a polycrystalline silicon thin film transistor according to the related art;

**[0040]** FIG. 4 is a schematic perspective view of a liquid crystal display device according to the related art;

**[0041]** FIG. 5 is a schematic circuit diagram illustrating one pixel of a liquid crystal display device according to the related art;

**[0042]** FIG. 6A is a schematic circuit diagram illustrating a stabilizing method including a first OFF-state stress applied to a liquid crystal display device according to the related art;

**[0043]** FIG. 6B is a timing chart illustrating a stabilizing method including a first OFF-state stress applied to a liquid crystal display device according to the related art;

**[0044]** FIG. 6C is a schematic cross-sectional view illustrating an effect of a first OFF-state stress of a stabilizing method according to the related art;

**[0045]** FIG. 6D is a current-voltage (I-V) curve illustrating an OFF-current of a P-TFT after a first OFF-state stress of a stabilizing method according to the related art;

**[0046]** FIG. 7A is a schematic circuit diagram illustrating a stabilizing method including a second OFF-state stress applied to a liquid crystal display device according to the related art;

**[0047]** FIG. 7B is a timing chart illustrating a stabilizing method including a second OFF-state stress applied to a liquid crystal display device according to the related art;

**[0048]** FIG. 7C is a schematic cross-sectional view illustrating an effect of a second OFF-state stress of a stabilizing method according to the related art;

**[0049]** FIG. 7D is a current-voltage (I-V) curve illustrating an OFF-current of a P-TFT after a second OFF-state stress of a stabilizing method according to the related art;

**[0050]** FIG. 8A is a schematic block diagram illustrating an apparatus for applying an OFF-state stress according to an embodiment of the present invention;

**[0051]** FIG. 8B is a schematic cross-sectional view taken along a line "VIIIB-VIIIB" of FIG. 8A;

**[0052]** FIG. 9 is a schematic block diagram illustrating a panel loading unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention;

**[0053]** FIG. 10A is a schematic block diagram illustrating a plurality of voltage control channels of a voltage control unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention;

**[0054]** FIG. 10B is a schematic block diagram illustrating a data terminal ground channel of a voltage control unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention; and

**[0055]** FIG. 11 is a schematic block diagram illustrating a panel selecting unit and a backlight selecting unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention.

## DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

**[0056]** Reference will now be made in detail to embodiments of the present invention, example of which is illustrated in the accompanying drawings. Wherever possible,

similar reference numbers will be used throughout the drawings to refer to the same or like parts.

**[0057]** FIG. 8A is a schematic block diagram illustrating an apparatus for applying an OFF-state stress according to an embodiment of the present invention and FIG. 8B is a schematic cross-sectional view taken along a line "VIIIB-VIIIB" of FIG. 8A.

**[0058]** In FIGs. 8A and 8B, an apparatus for applying an OFF-state stress includes a power supply unit 120, a panel loading unit 110, a voltage control unit 130, a frequency control unit 140, a time setting unit 150, a panel selecting unit 160, and a backlight selecting unit 170. The power supply unit 120 applies a source power, and the panel loading unit 110 includes panel jigs 111. An array substrate for an LCD device or an LCD panel 210 including attached substrates is loaded on each panel jig 111, and each panel jig 111 has a plurality of power input terminals 111a, 111b and 111c through which the source power is applied to the array substrate or the LCD panel 210. The voltage control unit 130 includes a plurality of voltage control channels 131, 132 and 133 that modulate a voltage of the source power and supply the voltage-modulated source power to the plurality of power input terminals 111a, 111b and 111c. The frequency control unit 140 modulates a frequency of the source power. The time setting unit 150 sets a time period for supplying the source power. The panel selecting unit 160 includes a plurality of panel selecting channels 161 that control supplying the source power to each panel jig 111. The backlight selecting unit 170 includes a plurality of backlight selecting channels 171 that control supplying a backlight source power to each panel jig 111.

**[0059]** FIG. 9 is a schematic block diagram illustrating a panel loading unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention.

**[0060]** In FIG. 9, a panel loading unit 110 includes a plurality of panel jigs 111. An array substrate for an LCD device or an LCD panel 210 (see FIG. 8A) may be loaded on each panel jig 111. Each panel jig 111 can be replaced on the panel loading unit 110 according to a size of the LCD device, for example, 3.7 inch, 4 inch and 4.6 inch, etc. In addition, each panel jig 111 includes first to third power input terminals 111a to 111c (see FIG. 8). A source power is applied to a gate line through the first power input terminal 111a and applied to a data line through the second power input terminal 111b. The source power is applied to a common line and a common electrode through the third power input terminal 111c. When the array substrate or the LCD panel 210 is loaded on the panel jig 111, the first, second and third power input terminals 111a, 111b and 111c contact a gate pad 210a (see FIG. 8B) connected to the gate line, a data pad 210b (see FIG. 8B) connected to the data line and a common pad 210c (see FIG. 8B) connected to the common line and the common electrode, respectively. The first to third power input terminals 111a, 111b and 111c can be disposed at a specific position according to a position of pads 210a, 210b and 210c of the array substrate or the LCD panel 210.

**[0061]** FIG. 10A is a schematic block diagram illustrating a plurality of voltage control channels of a voltage control unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention. FIG. 10B is a schematic block diagram illustrating a data terminal ground channel of a voltage control unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention.

**[0062]** The voltage control unit of FIGs. 10A and 10B may include a gate voltage control channel 131 (of FIG. 8), a data voltage control channel 132, a common voltage control channel 133, a data terminal ground channel 134 and a monitor indicating an modulated value of voltage. The gate voltage control channel 131 (of FIG. 8) modulates and supplies a gate voltage to a gate pad through a first power input terminal 111a (of FIG. 8) of a panel jig 111 (of FIG. 8). The data voltage control channel 132 modulates and supplies a data voltage to a data pad through a second power input terminal 111b (of FIG. 8). The common voltage control channel 133 modulates and supplies a common voltage to a common pad through a third power input terminal 111c (of FIG. 8). The data terminal ground channel 134 keeps a voltage of a pad grounded. The voltage control unit may further include additional voltage control channels according to a kind of source power supplied to the panel jig 111 (of FIG. 8) and application.

**[0063]** Referring again to FIG. 8, the frequency control unit 140 includes a gate frequency control channel 141, a data frequency control channel 142 and a common frequency control channel 143 to modulate a frequency of an AC (alternating current) voltage supplied to each of the plurality of power input terminals 111a, 111b and 111c of the panel jig 111 through each of the plurality of voltage control channels 131, 132 and 133 of the voltage control unit 130. The gate frequency control channel 141 modulates a frequency of a gate voltage supplied through a gate voltage control channel 131; and the data frequency control channel 142 modulates a frequency of a data voltage supplied through a data voltage control channel 132. The common frequency control channel 141 modulates a frequency of a common voltage supplied through a common voltage control channel 133. Therefore, each of the gate voltage, the data voltage and the common voltage becomes an AC voltage having a

frequency, i.e., a pulse by the frequency control unit 140 and then supplied to the plurality of power input terminals 111a, 111b and 111c. The time setting unit 150 functions as a timer for setting a time period of supplying the source power through the voltage control unit 130.

**[0064]** FIG. 11 is a schematic block diagram illustrating a panel selecting unit and a backlight selecting unit of an apparatus for applying an OFF-state stress according to an embodiment of the present invention.

**[0065]** In FIG. 11, a panel selecting unit 160 determines one panel jig 111 to which a source power is supplied. The panel selecting unit 160 includes a plurality of panel selecting channels 161 functioning as an ON/OFF switch and corresponding to the plurality of panel jigs 111. The backlight selecting unit 170 also determines one panel jig 111 to which a backlight source power is supplied. As a result, the backlight selecting unit 170 includes a plurality of backlight selecting channels 171 functioning as an ON/OFF switch and corresponding to the plurality of panel jigs 111.

**[0066]** An operation of an apparatus for applying an OFF-state stress will be illustrated.

**[0067]** Referring again FIG. 8, an array substrate for an LCD device or an LCD panel is loaded on one panel jig 111. First, second and third power input terminals 111a, 111b and 111c of the panel jig 111 are connected to a gate pad, a data pad and a common pad of the array substrate or the LCD panel, respectively. Next, a source power including a gate voltage, a data voltage and a common voltage is supplied from a power supply unit 120. A gate voltage control channel 131, a data voltage control channel 132 and a common voltage control channel 133 of a voltage control unit 130 modulate a voltage of the source power, and a data terminal ground channel 134 determines whether the data pad is grounded or not.

After modulating the voltage of the source power, a frequency control unit 140 adds an AC voltage to the voltage-modulated source power through a frequency control channel. Next, after selecting a panel jig 111, a panel selecting channel 161 of a panel selecting unit 160 is turned ON. When an LCD panel is loaded on the panel jig 111, a backlight selecting channel 171 of a backlight selecting unit 170 may be turned ON to supply a backlight source power for testing a backlight unit. Next, after setting a time period of supplying the source power, a stabilization process for a P-TFT is performed by applying an OFF-state stress.

**[0068]** Since an apparatus for applying an OFF-state stress to a P-TFT uses an AC voltage, the apparatus has a simpler structure and an higher stabilization effect. Accordingly, residual images can be reduced by an OFF-current reduction. Moreover, since the apparatus performs the stabilization process for a plurality of panels at the same time by expansion of panel jigs, production yield can be improved.

**[0069]** It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.